北京大学
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人工智能与芯片设计

6- Design Flow II (AI for Chip中的必要背景概念)

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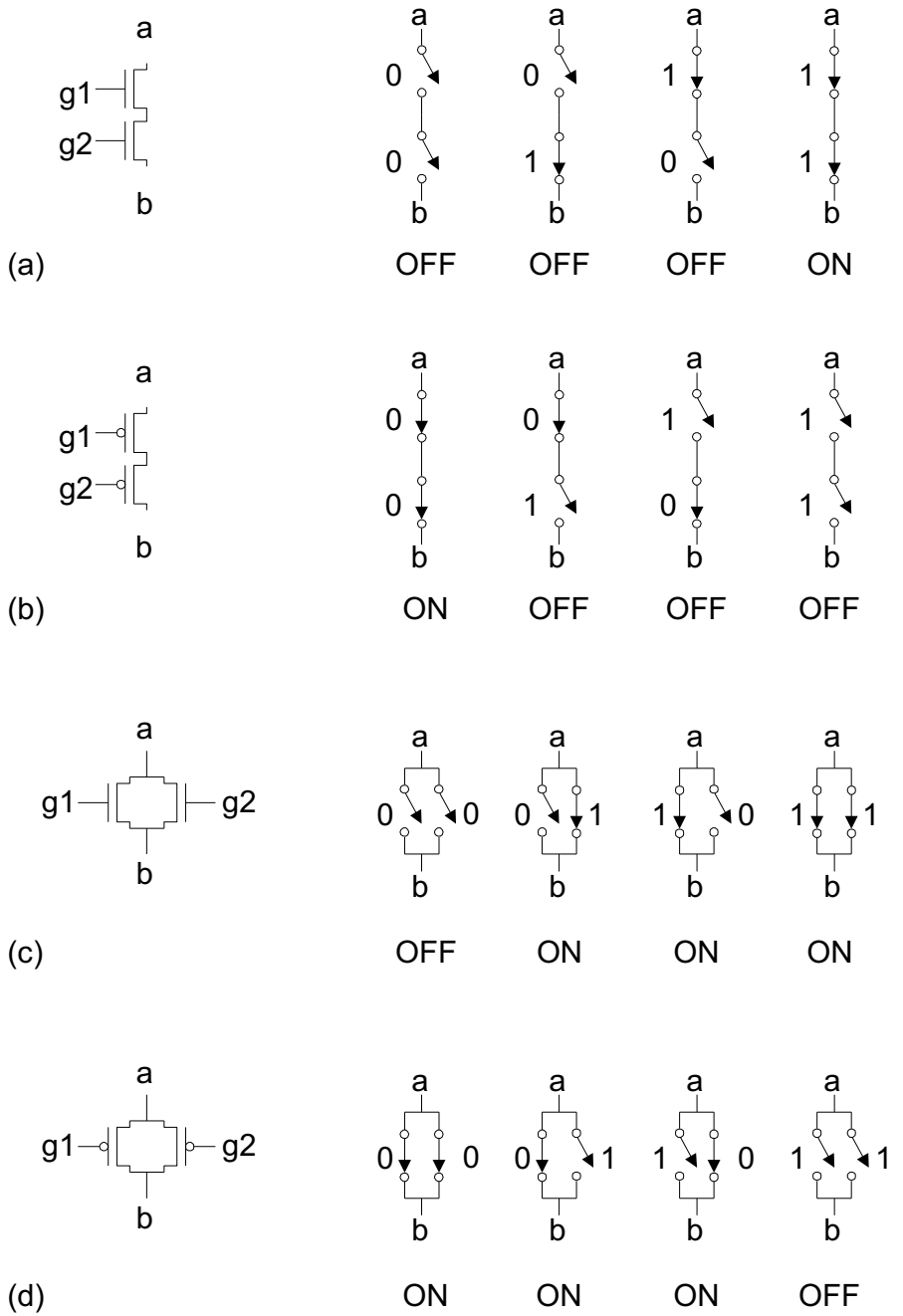
2023秋

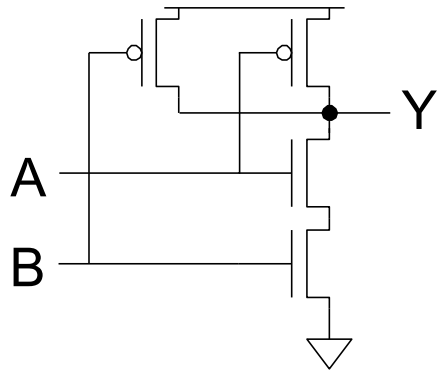
From Transistor to Gate

- nMOS: 1 = ON
- pMOS: 0 = ON
- *Series*: both must be ON
- *Parallel*: either can be ON



From Transistor to Gate

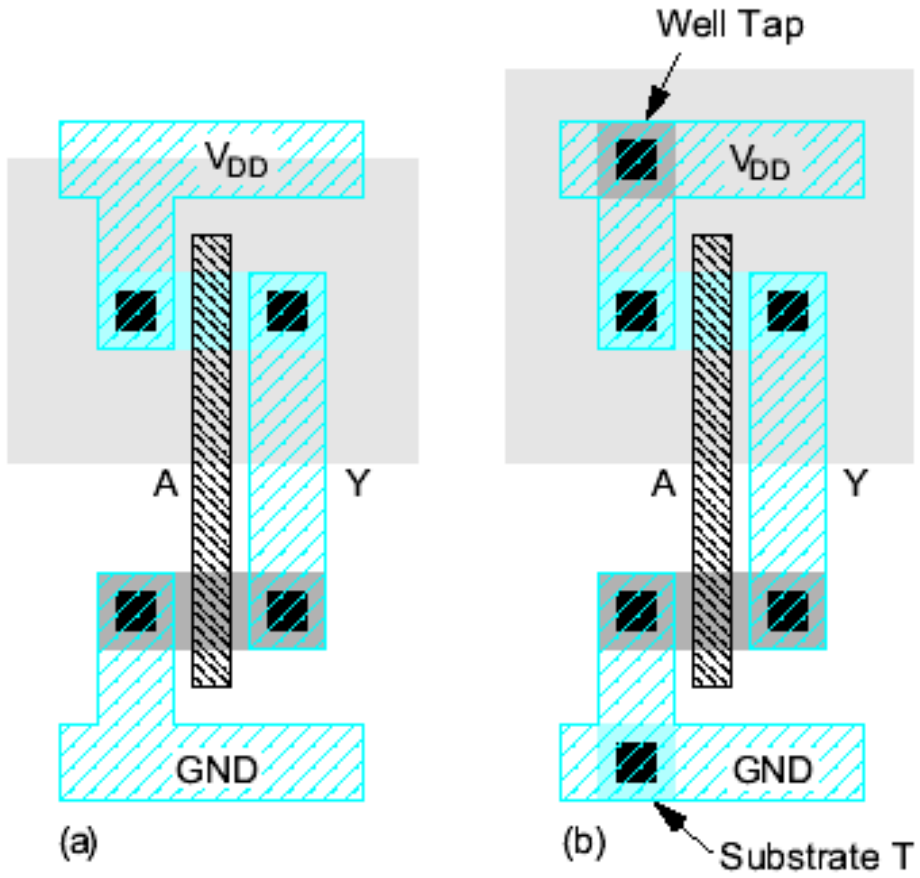
- Complementary CMOS gates always produce 0 or 1
- Ex: NAND gate
  - Series nMOS: Y=0 when both inputs are 1
  - Thus Y=1 when either input is 0
  - Requires parallel pMOS



- Rule of *Conduction Complements*
  - Pull-up network is complement of pull-down
  - Parallel -> series, series -> parallel

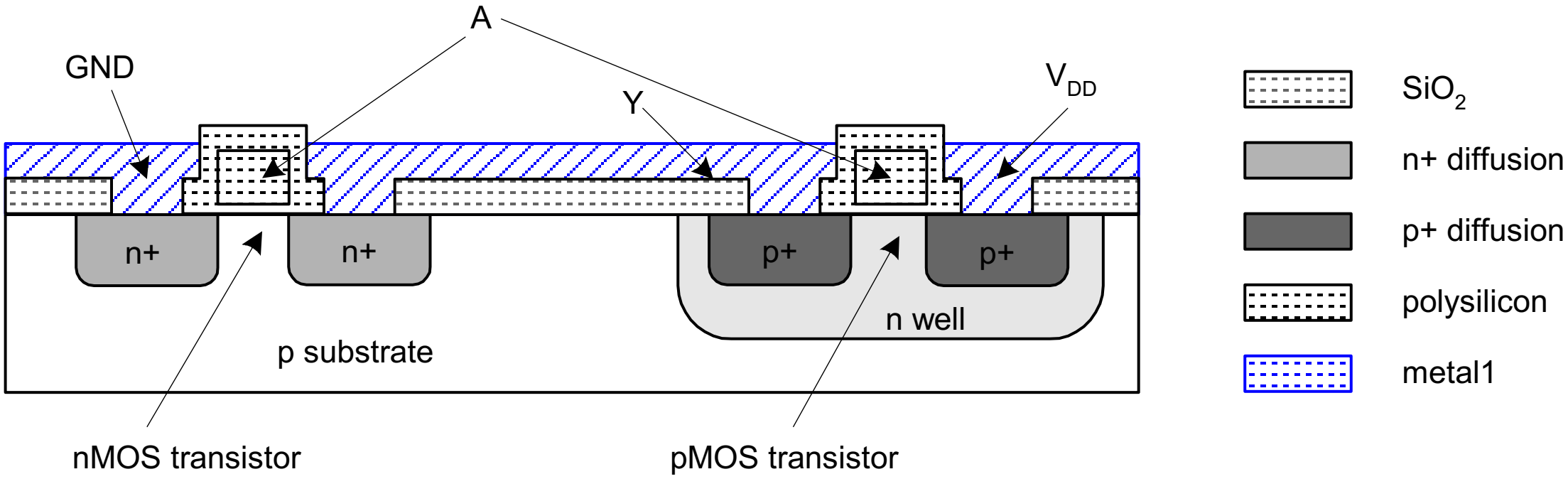
From Gate to Layout

- What are these?
  - Inverter Layout



Inverter Cross-section

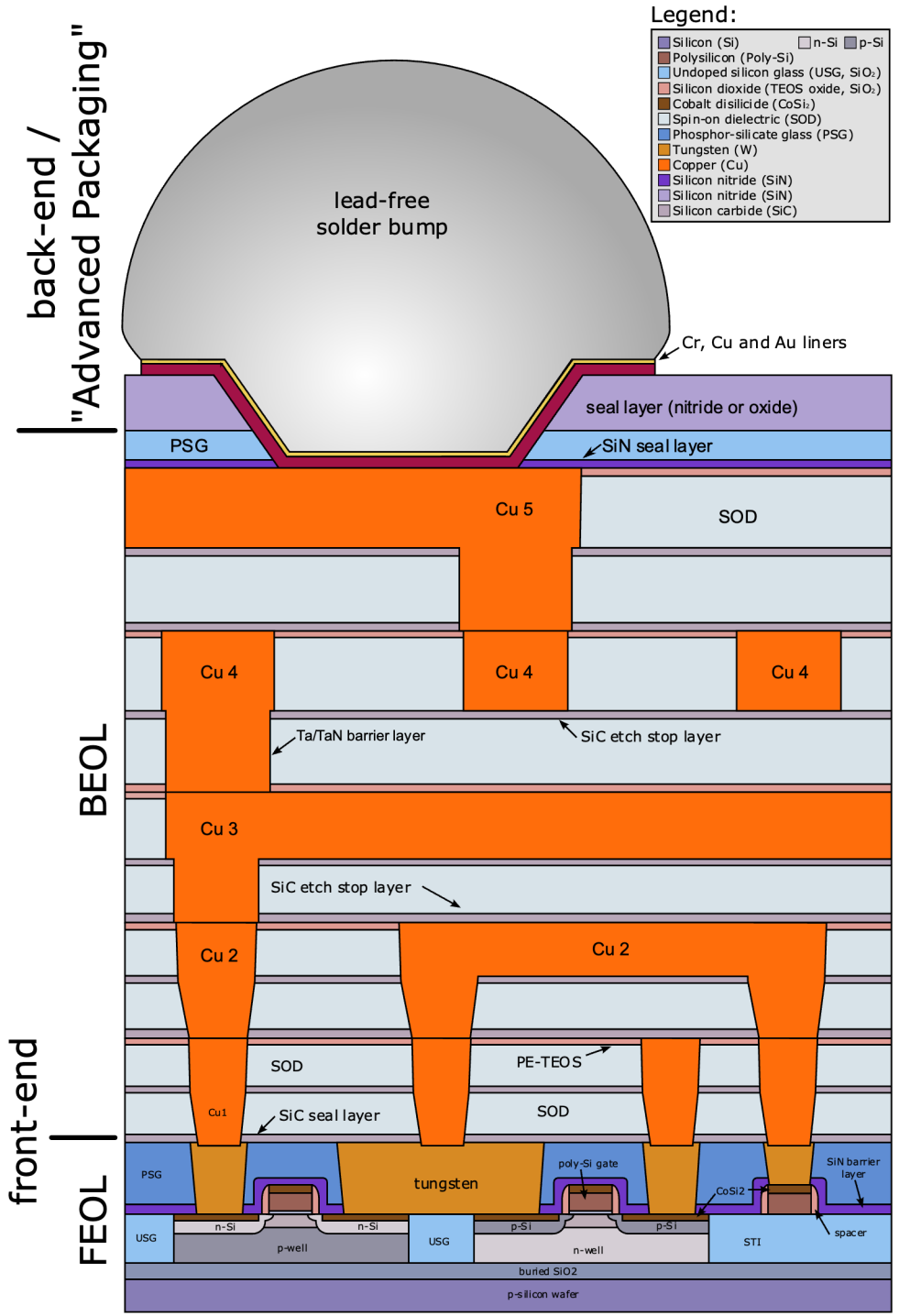
- Typically use p-type substrate for nMOS transistors
- Requires n-well for body of pMOS transistors



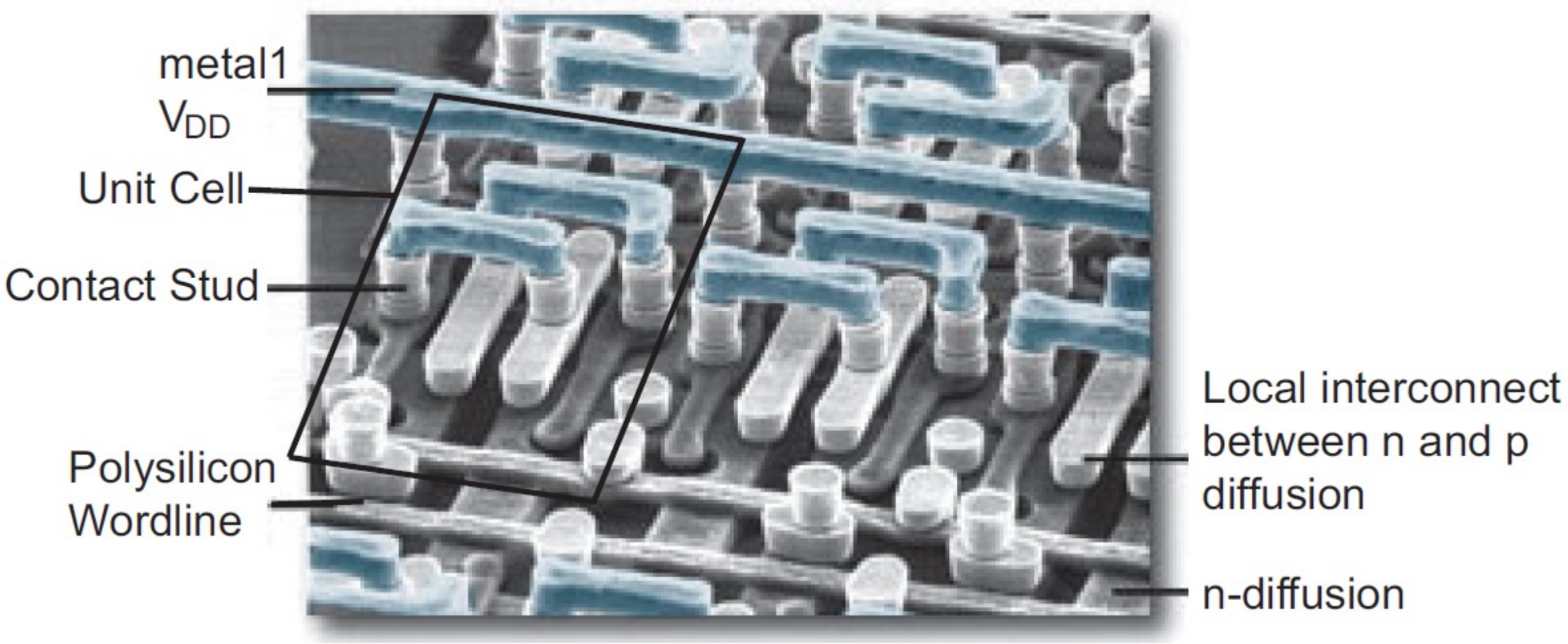
BEOL Layer Stack

- BEOL: back-end-of-line
- FEOL: front-end-of-line

- Where are novel devices placed?

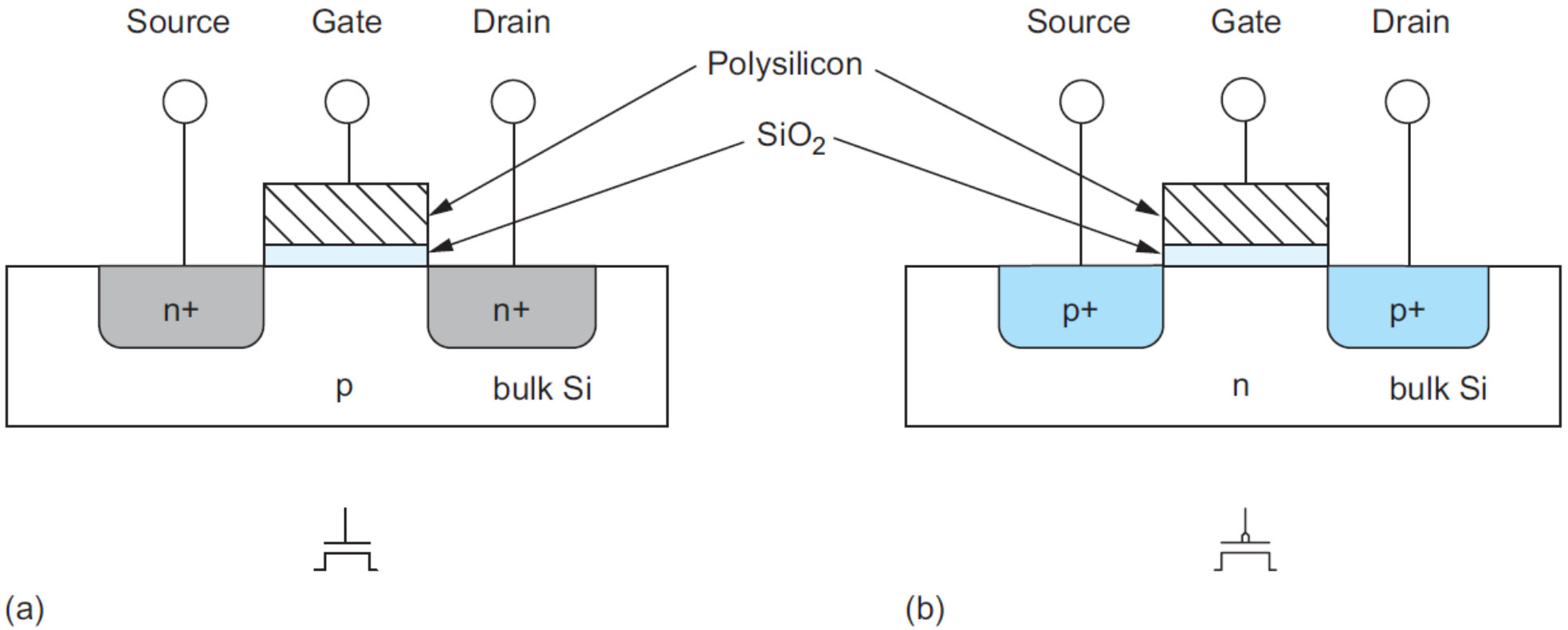


Interconnect



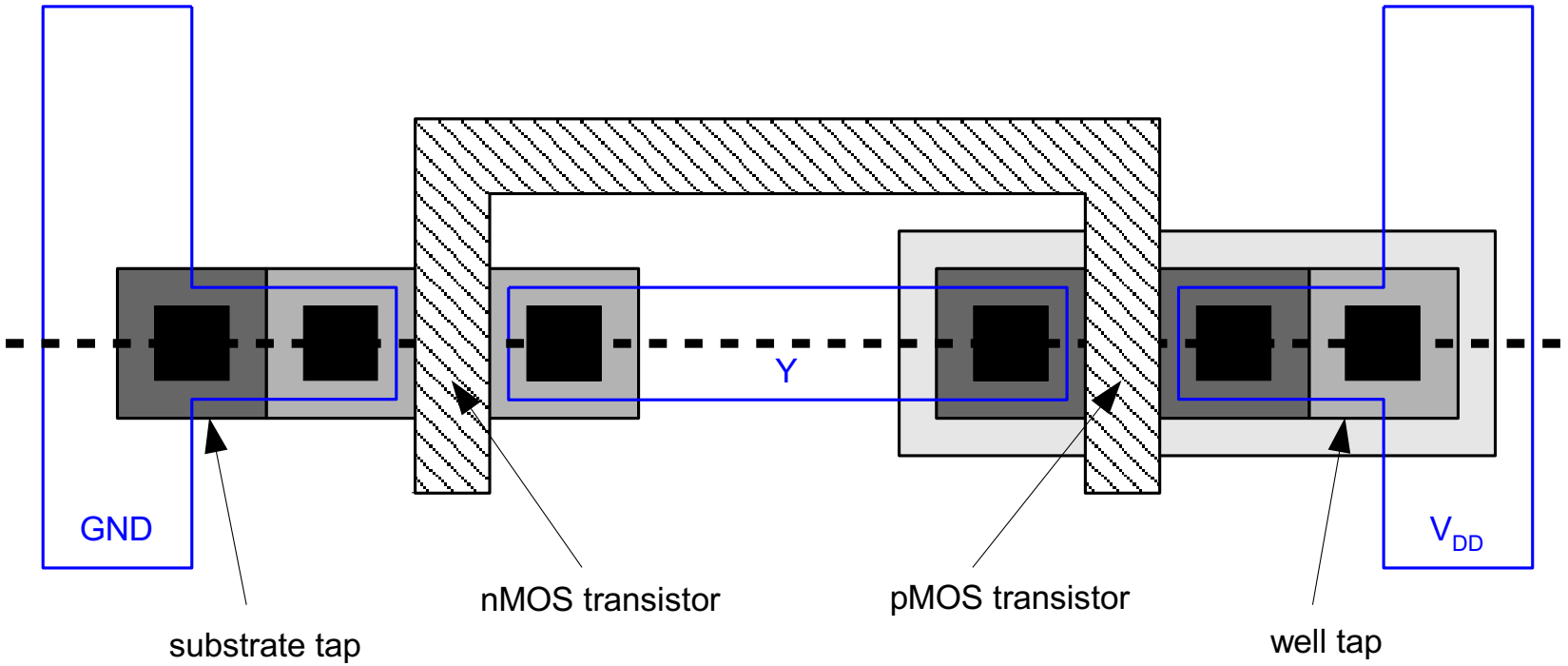
Inverter Cross-section

- Device to Symbol



Inverter Mask Set

- Transistors and wires are defined by *masks*
- Cross-section taken along dashed line



From Gate to Layout

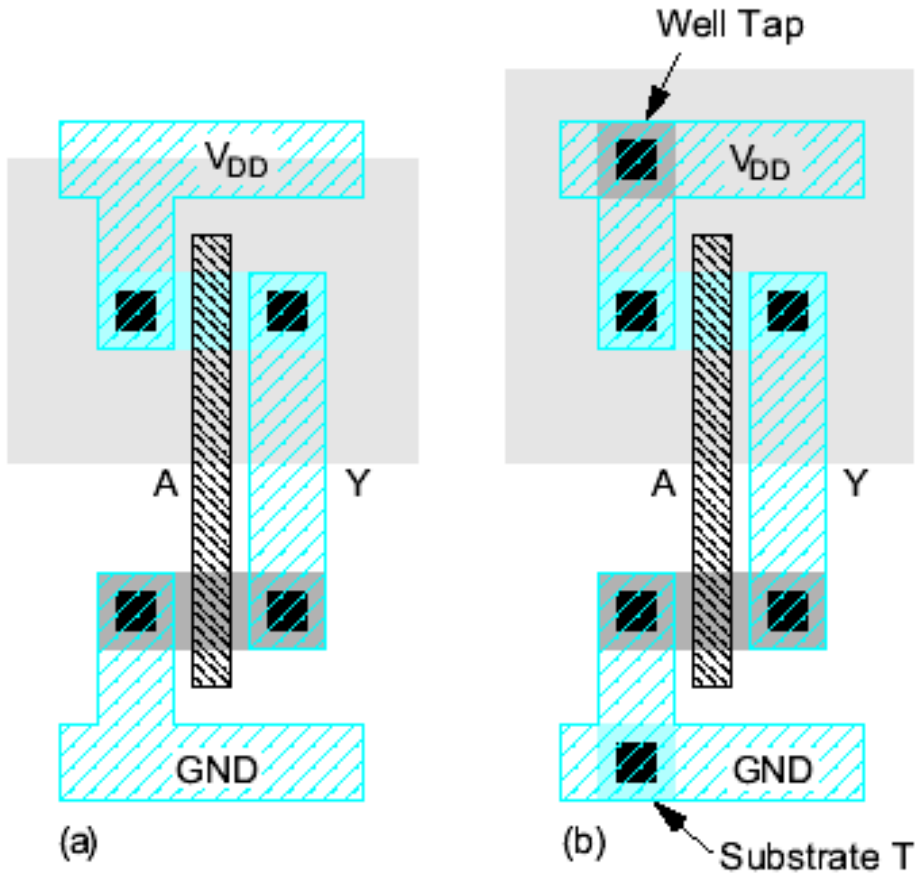
- What are these?
  - Inverter Layout

SPICE netlist

```
MP1 (Y A VDD VDD) PMOS
MN1 (Y A GND GND) NMOS
```

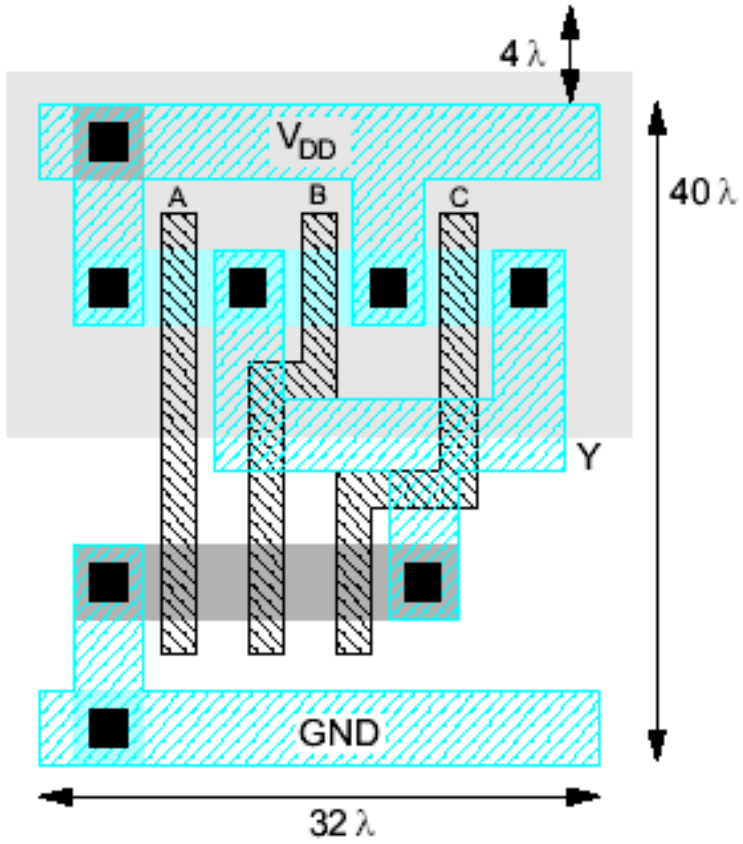
Verilog netlist

```
Inverter u1 (.in(A), .out(Y))
```



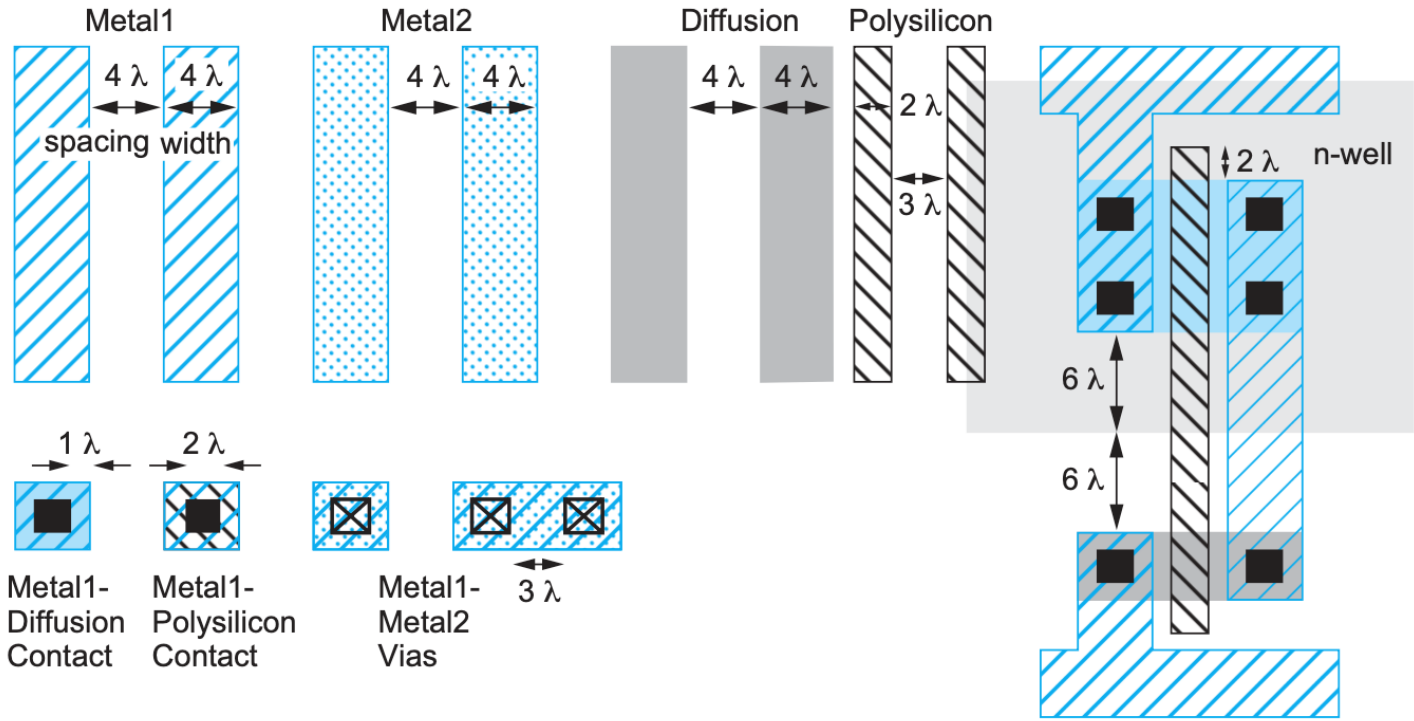
From Gate to Layout

- Horizontal N-diffusion and p-diffusion strips
- Vertical polysilicon gates
- Metal1 V_{DD} rail at top
- Metal1 GND rail at bottom
- 32 λ by 40 λ



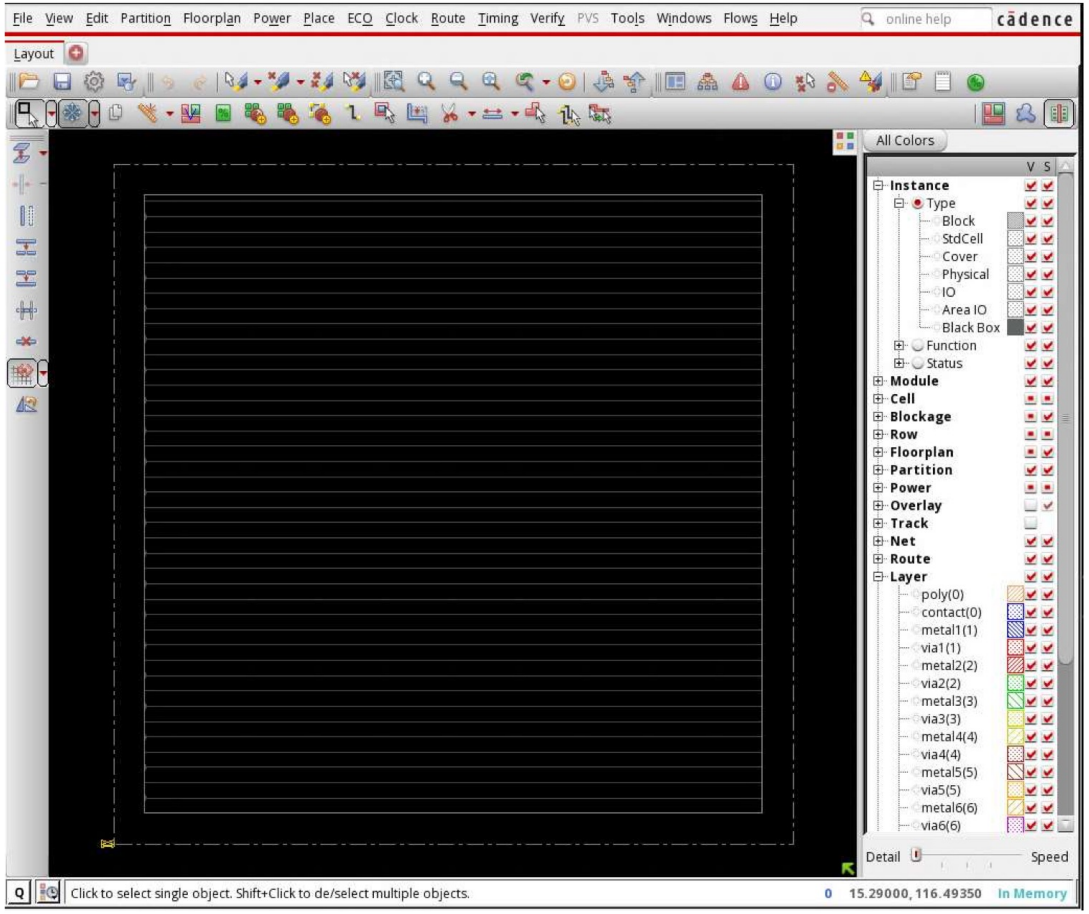
Design Rule Check

Layer	Rule	Description	65 nm Rule (μm)
Well	1.1	Width	0.5
	1.2	Spacing to well at different potential	0.7
	1.3	Spacing to well at same potential	0.7
Active (diffusion)	2.1	Width	0.10
	2.2	Spacing to active	0.12
	2.3	Source/drain surround by well	0.15
	2.4	Substrate/well contact surround by well	0.15
	2.5	Spacing to active of opposite type	0.25
Poly	3.1	Width	0.065
	3.2	Spacing to poly over field oxide	0.10
	3.2a	Spacing to poly over active	0.10
	3.3	Gate extension beyond active	0.10
	3.4	Active extension beyond poly	0.10
	3.5	Spacing of poly to active	0.07

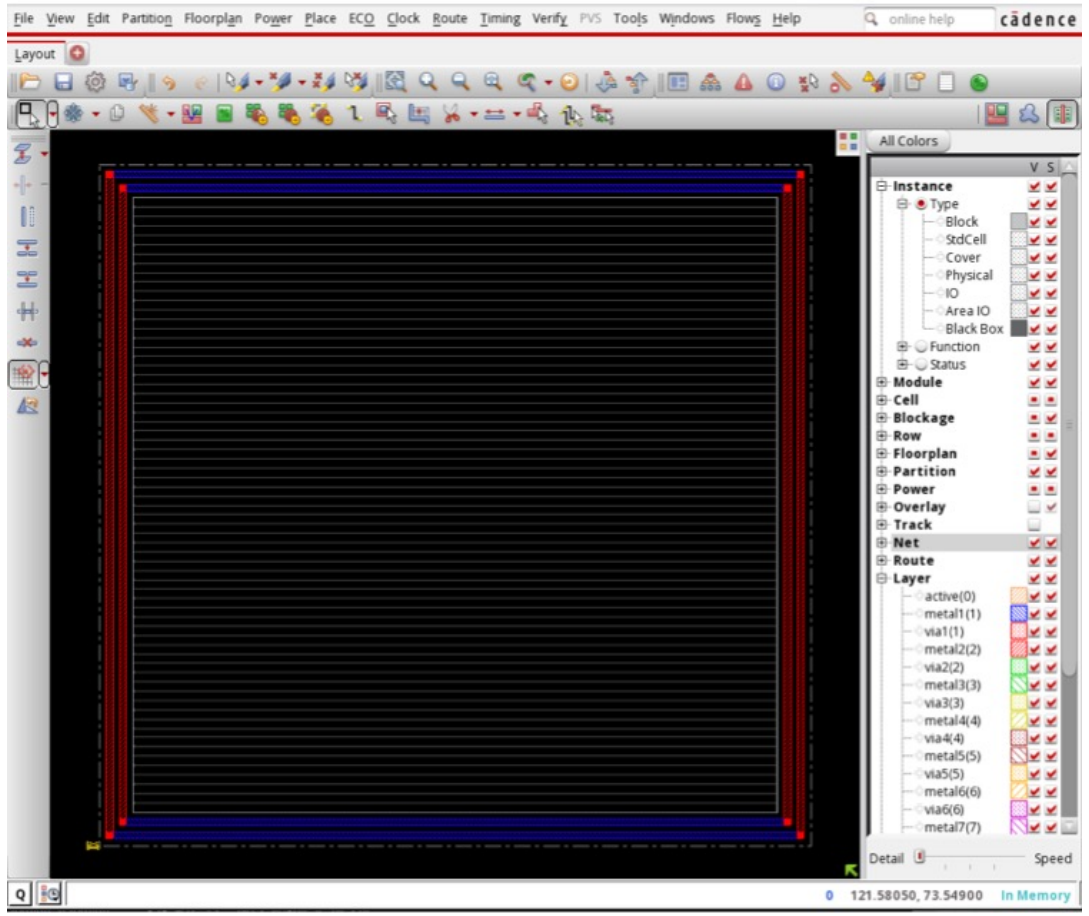


Example of Back-end Design (Physical Design)

Initial



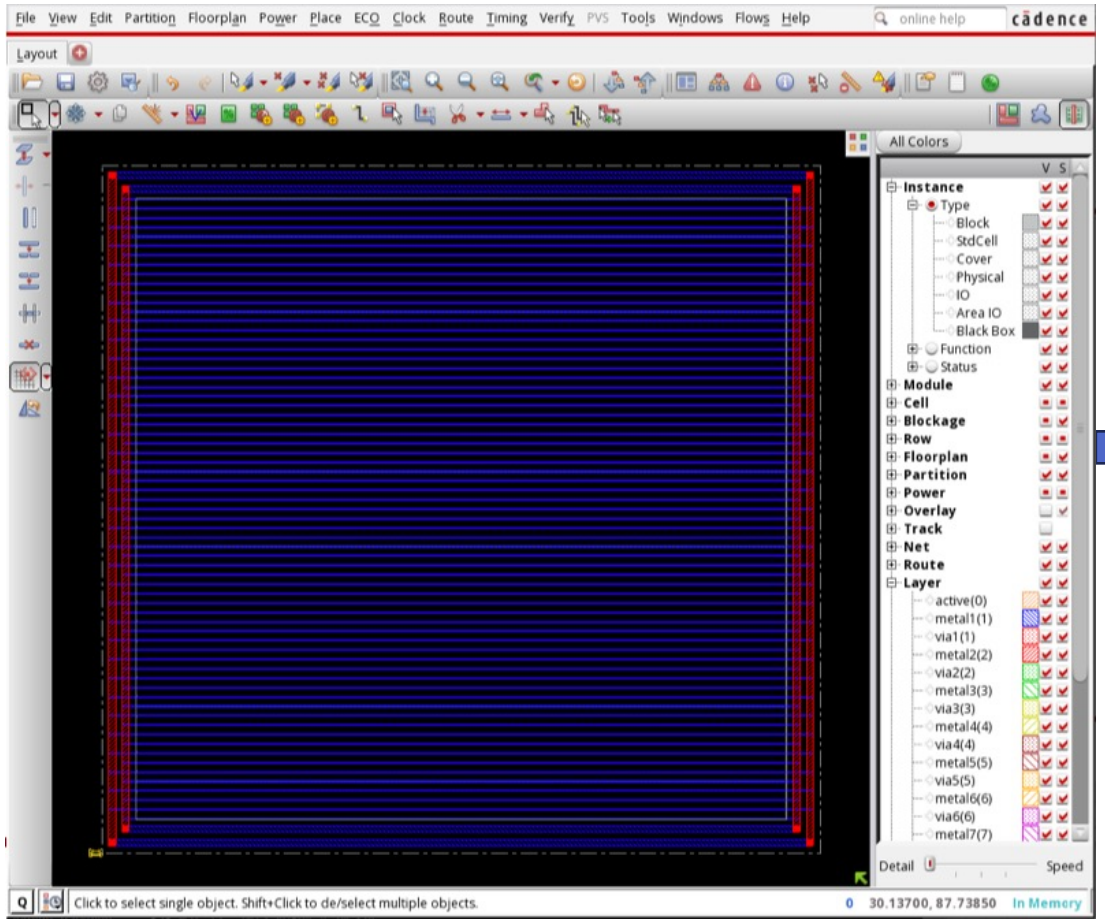
Place Power Ring

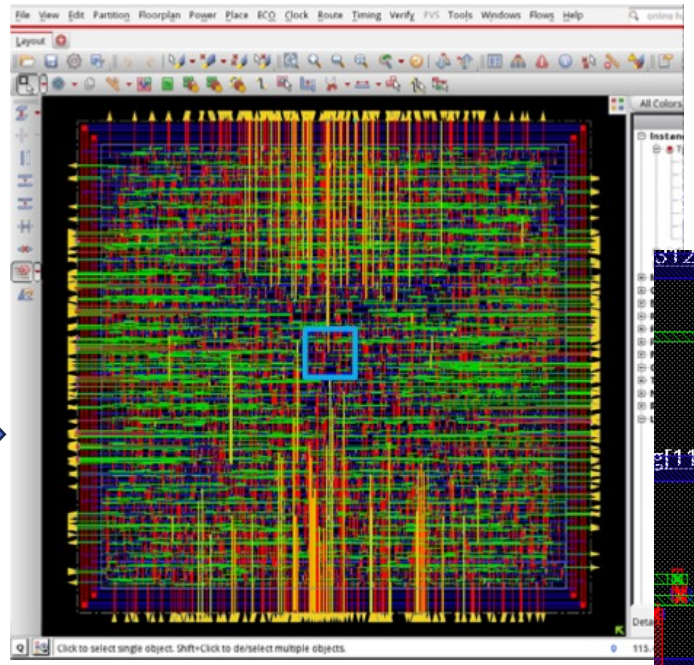


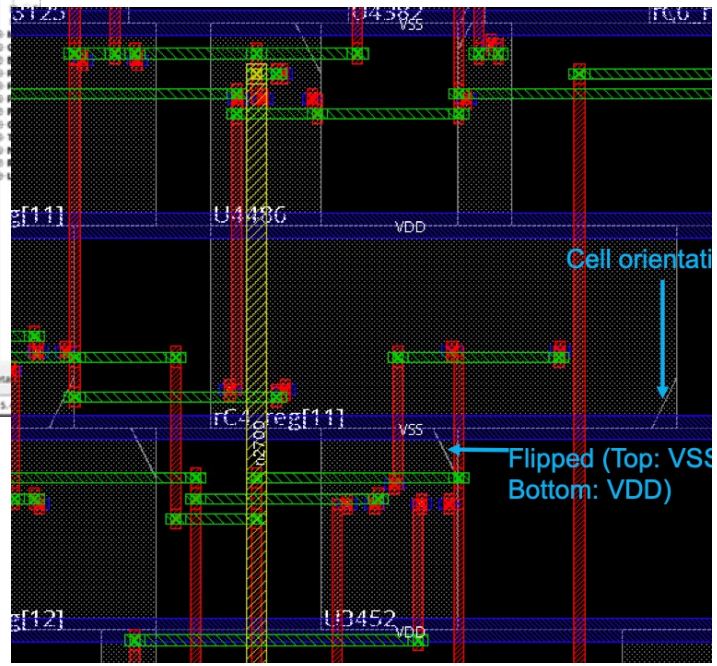
Example of Back-end Design (Physical Design)

Place Power Rail

Place Power Ring

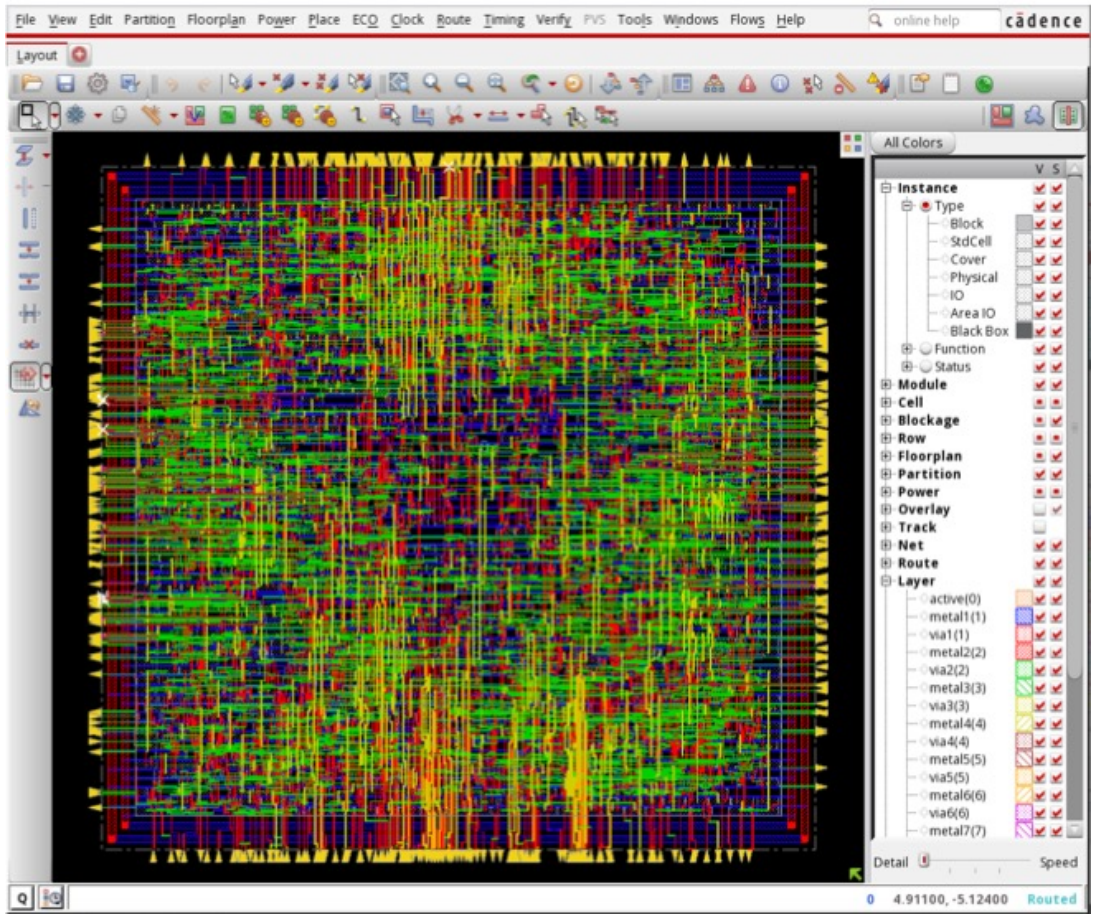






Example of Back-end Design (Physical Design)

Routing



Full-Chip Layout (Courtesy: Bonan Yan's Group)